REMARKS

By entry of this amendment, claims 7-17 are pending in this application. Claims 7-16 have been amended, and claim 17 is new. No new matter has been added.

Claim Rejections under 35 U.S.C. § 102

Claims 7-9 stand rejected under 35 U.S.C. §102(b) as allegedly being anticipated by Uenishi et al. (U.S. Patent No. 5,894,149). Applicants respectfully disagree.

In making the rejection, the Office cites various elements of FIG. 30 of Uenishi as disclosing features of claimed embodiments. For example, the Office cites element 70 as disclosing the claimed trench gate. The Office further cites element 70 as meeting the claimed feature of the trench gate extends along a longitudinal direction and the width of the trench gate varies along the longitudinal direction. As best understood by the Applicants, the word "longitudinal" refers to the length of the claimed semiconductor device. As shown in Applicants' FIGS. 1 and 2, the "longitudinal direction" is along the x-axis. In contrast, Uenishi's element 70 as shown in FIG. 30 as well as FIGS. 39 and 42-49 does not vary in either a longitudinal or lateral direction within a semiconductor device. Uenishi illustrates element 70, a trench gate, adjacent to an emitter trench, element 80, in FIG. 30. As shown in FIG. 30, the width of the emitter trench (element 80) differs from the width of the trench gate (element 70), and the width of element 70, which appears to be on another side of element 80, is constant.

In addition, Applicants have further refined the claim to recite a portion of the intermediate region facing the gate isolates the top region and the deep region. In making the rejection, the Office asserts that the trench gate 70 of Uenishi isolates the top region 5 from the deep region 1. However, in Applicants' FIG. 1, the top region 5 is separated from the deep region To more clearly distinguish these differences, Applicants have amended claim 7. Claim 7 now recites, in part:

> a trench gate facing a portion of the intermediate region via an insulating layer, wherein the portion ***of the intermediate region*** facing the trench gate isolates the top region and the deep region, and wherein ***the trench gate extends along a longitudinal direction in a plan view of the semiconductor device*** and ***width of the trench gate varies along the longitudinal direction in a plan view of the semiconductor device***.

Uenishi does not disclose the above highlighted features. Accordingly, Uenishi does not anticipate claim 7. Claims 8 and 9 recite an additional level of detail that also is not disclosed by Uenishi. Claims 8 and 9 also are not anticipated by Uenishi. Claims 7-9 are allowable.

Claim Rejections under 35 U.S.C. § 103

Claims 10-16 stand rejected under 35 U.S.C. §103(a) as allegedly being unpatentable over Uenishi et al. Applicants respectfully disagree.

Claims 10-16 depend ultimately from claim 7. Since Uenishi does not disclose all of the features recited in claim 7, Uenishi also does not recite all of the features in Applicants' claims 10-16.

In addition, claims 11, 13, 15 and 16 have been amended to further distinguish the varying width of the trench gate in the longitudinal direction. For example, claims 11 and 15 recite:

> wherein a pair comprising ***a wider width*** and ***a narrower width*** is repeated along the longitudinal direction ***in one trench gate***, and ***total length of the wider width along the longitudinal direction is 30 to 80 % of the total length of the trench gate along the longitudinal direction***.

These features are neither disclosed in nor rendered obvious by Uenishi. For example, Uenishi does not disclose of suggest a pair comprising a wider width and a narrower width that is repeated along the longitudinal direction in one trench gate. Accordingly, claims 11 and 15 are also allowable for this reason.

As for claims 13 and 16, these claims recite:

> wherein width of the intermediate region interposed between adjacent trench gates ***at wider width is narrow*** such that the intermediate region interposed between adjacent trench gates ***at wider width becomes a depressed region when on-voltage is not being applied to the trench gates***, and the top region is located above the intermediate region ***interposed between adjacent trench gates at wider width***.

Uenishi does not such an intermediate region as recited in claims 13 and 16. Claims 13 and 16 recite an additional level of detail that is neither disclosed nor suggested by Uenishi. Accordingly, claims 13 and 16 are also allowable for this reason.

Claim 17 is Allowable

Claim 17 is allowable for at least the same reasons as claim 7 above. Claim 17 recites, in part:

> a trench gate ***extending through the top region and having a gate electrode***, the trench gate further facing a portion of the intermediate region via an insulating layer, wherein the portion of the intermediate region facing the trench gate isolates the top region and the deep region, and ***wherein the trench gate further extends along a longitudinal direction in a plan view of the semiconductor device and width of the trench gate varies along the longitudinal direction in a plan view of the semiconductor device***.

Uenishi does not disclose the above highlighted features in combination with the other features recited in claim 17. Accordingly, claim 17 is allowable.

Conclusion

All outstanding rejections have been overcome. It is respectfully submitted that, in view of the foregoing amendments and remarks, the application is in clear condition for allowance. Issuance of a Notice of Allowance is earnestly solicited.

Although not believed necessary, the Office is hereby authorized to charge any fees required under 37 C.F.R. § 1.16 or § 1.17 or credit any overpayments to Deposit Account No. 11-0600.

The Office is invited to contact the undersigned at 202-220-4200 to discuss any matter regarding this application.

Date: April 30, 2009

/Martin E. Miller/
Martin E. Miller
Registration No. 56,022

Kenyon & Kenyon LLP
1500 K Street, NW, Suite 700
Washington, DC 20005-1257
Tel.: (202) 220-4200
Fax.: (202) 220-4201